Parameterized Complexity via Combinatorial Circuits (Extended Abstract)

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ABSTRACT. The classes of the W-hierarchy are the most important classes of intractable problems in parameterized complexity. These classes were originally defined via the weighted satisfiability problem for Boolean circuits. The analysis of the parameterized majority vertex cover problem and other parameterized problems led us to study circuits that contain connectives such as *majority*, *not-all-equal*, and *unique*, instead of (or in addition to) the Boolean connectives. For example, a gate labelled by the majority connective outputs TRUE if more than half of the inputs are TRUE. For any finite set $\mathcal{C}$ of connectives we construct the corresponding W($\mathcal{C}$)-hierarchy. We derive some general conditions which guarantee that the W-hierarchy and the W($\mathcal{C}$)-hierarchy coincide levelwise. Surprisingly, if $\mathcal{C}$ contains *only* the majority connective (i.e., no boolean connectives), then the first levels coincide. We use this to show that the majority vertex cover problem is W$[1]$-complete.

1 Introduction

Parameterized complexity is a refinement of classical complexity theory, in which one takes into account not only the total input length n, but also other aspects of the problem codified as the parameter k. In doing so, one attempts to confine the exponential running time needed for solving many natural problems strictly to the parameter. For example, the classical VERTEX-COVER problem can be solved in $O(2^k \cdot n)$ time, when parameterized by the size k of the solution sought [8] (significant improvements to this algorithm are surveyed in [9]). This running time is practical for instances with small parameter, and in general is far better than the $O(n^{k+1})$ running time of the brute-force algorithm. More generally, a problem is said to be *fixed-parameter tractable* if it has an algorithm running in time $f(k) \cdot p(n)$, where n is the length of the input, k its parameter, f an arbitrary

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computable function and p a polynomial. Such an algorithm is said to run in *fpt-time*, and FPT denotes the class of all parameterized problems that are fixed-parameter tractable.

Parameterized complexity theory not only provides methods for proving problems to be fixed-parameter tractable but also gives a framework for dealing with apparently intractable problems. There is a great variety of classes of parameterized intractable problems. However, the most important of these classes are the classes W$[1]$, W$[2]$,... of the W-hierarchy, on top of which there are the classes W[SAT] and W[P],

$$\text{FPT} \subseteq \text{W}[1] \subseteq \text{W}[2] \subseteq \cdots \subseteq \cdots \subseteq \text{W[SAT]} \subseteq \text{W[P]}.$$

These classes were originally defined via the weighted satisfiability problem for Boolean circuits. In this context Boolean circuits are allowed to contain NOT gates, *small* AND and OR gates of fan-in ≤ 2 and *large* AND and OR gates of arbitrary finite fan-in. The *weft* of such a circuit is the maximum number of large gates on a path from an input to the output, its *depth* the maximum number of all gates on a path from an input to the output. The (Hamming) *weight* of an assignment of truth values to the input variables of the circuit is the number of variables set to TRUE. A circuit is *k-satisfiable* if there is an assignment of weight k satisfying it. The *parameterized weighted satisfiability problem* p-WSAT(Ω) for a class Ω of circuits is the problem

p-WSAT(Ω)	
Input:	A circuit D in Ω and a natural number k.
Parameter:	k.
Question:	Is D k-satisfiable?

By definition W$[t]$ is the class of parameterized problems reducible to p-WSAT$(\Omega_{t,d})$ for some $d \geq 1$, where $\Omega_{t,d}$ is the class of Boolean circuits of weft $\leq t$ and depth $\leq d$. Using this definition one easily verifies that the parameterized clique problem p-CLIQUE (when parameterized by the size of the solution sought) is in W$[1]$ and that the parameterized dominating set problem p-DOMINATING-SET is in W$[2]$. In fact, these problems are complete problems for W$[1]$ and W$[2]$, respectively.

Some problems suggest to analyze circuits with other types of gates. For example, let us consider the parameterized problem

p-MAJORITY-VERTEX-COVER	
Input:	A graph $G = (V, E)$ and $k \in \mathbb{N}$.
Parameter:	k.
Question:	Is there a set of k vertices in G which covers a majority of the edges of G, i.e., is there $S \subseteq V$ with $\lvert S\rvert = k$ and $\lvert\{e \in E \mid e \cap S \neq \emptyset\}\rvert > \lvert E\rvert/2$?

It is not hard to reduce this problem to the weighted satisfiability problem for majority circuits of weft 1 and depth 2 (see Section 5). The gates of such a circuit are majority gates, that is, they are labelled by the connective *Maj*, which outputs TRUE if more than half of its inputs are TRUE. Such a gate is *small* if it has fan-in ≤ 3. What is the information that we can get out of this? This paper addresses questions of this kind.

Besides the majority connective there are other quite natural connectives. We mention the connectives

NAE (*not-all-equal*)	(there are inputs set to TRUE and inputs set to FALSE)
U (*unique*)	(exactly one input is set to TRUE)
$c_>$	(at most $c-1$ inputs are set to TRUE).
$c_\leq$	(at least c inputs are set to TRUE)

(here we assume that c is a natural number ≥ 1). We call the connectives $c_>$ and $c_\leq$ the *threshold connectives*.

The connective *NAE* has the property that if we find an input set to TRUE and one set to FALSE the value of an *NAE*-gate will be TRUE no matter what the truth values of the other inputs are. Also the connectives U, $c_>$, and $c_\leq$ have the property that a "bounded number of inputs determine the value". The majority connective *Maj* does not have this property. We call connectives C which share the property *bounded* in Section 2. The corresponding bound determines what should be called a small C-gate. This allows to define the W(C)-hierarchy in just the same way as the W-hierarchy was defined. Using the boundedness it is not hard to show that the W(C)-hierarchy is contained levelwise in the W-hierarchy.

The following observation leads to the reverse inclusion. A Π_t Boolean circuit as defined by Sipser [10] consists of t levels of large gates that alternate AND and OR with an AND gate at the top and with the bottom level gates connected to the input variables and their negations. Such a circuit is in Π_t^+ if negations do not occur and in Π_t^- if all variables are negated. It is well-known [4] that

- if t is even, then p-WSAT(Π_t^+) is complete for W$[t]$;
- if $t > 1$ is odd, then p-WSAT(Π_t^-) is complete for W$[t]$.

Let $t > 1$. Circuits in Π_t^+ (if t is even) or in Π_t^- (if t is odd), written as propositional formulas, have the form

(1) $$\neg \bigvee_{i_1} \neg \bigvee_{i_2} \cdots \neg \bigvee_{i_t} Y_{i_1 \dots i_t}$$

with variables $Y_{i_1 \dots i_t}$. Let C_0 be the connective "defined" by the equivalence

$$C_0[Y_1, \dots, Y_n] \equiv \neg \bigvee_{i \in [n]} Y_i.$$

Then (1) shows that for every connective C "capable to simulate the connective C_0 by a circuit of weft 1 and of constant depth" the W(C)-hierarchy will contain the W-hierarchy levelwise. This applies to the connectives *NAE*, U, and $c_>$. We prove this result in a more general framework in Section 3.

In Section 4 we deal with the connective $c_\leq$. The picture we gain is quite different. For fixed depth the weighted satisfiability problem is solvable in polynomial time. The parameterized weighted satisfiability problem for such circuits is

- W$[1]$-complete if the depth is bounded in terms of the parameter;
- W[SAT]-complete if the depth is logarithmic in the circuit size;
- W[P]-complete for circuits of arbitrary depth.

Finally, in Section 5 we deal with the majority connective *Maj*. We show that the W-hierarchy is contained levelwise in the W(*Maj*)-hierarchy. While we conjecture that W$[t] \subset$ W$[t]$(*Maj*) for $t > 1$, we can show that the first levels coincide. We shall use this result to show that the problem p-MAJORITY-VERTEX-COVER is W$[1]$-complete.

As circuits only containing the connectives $c_\leq$ and *Maj* are monotone, by the previous results we get W[1]-complete weighted satisfiability problems of *monotone* circuits. Such problems for Boolean circuits are not known (however, compare [7]).

2 Bounded connectives and its W-hierarchy

The set of natural numbers is denoted by $\mathbb{N}$. For a natural number n let $[n] := \{1, \ldots, n\}$.

Contrary to the classical Boolean unary and binary connectives $\neg$, $\wedge$, and $\vee$ our connectives have no fixed arity.

Definition 1. *A* connective C *is a polynomial time computable binary function defined on all pairs* $(m, n) \in \mathbb{N} \times \mathbb{N}$ *with* $m + n \geq 1$ *and with values in* $\{1, 0\}$. [1]

We interpret $C(m, n) = 1$ as "C outputs a '1' (=TRUE), if it gets as input m-many '1's and n-many '0's." Examples of connectives are the *(big) conjunction* $\bigwedge$, the *(big) disjunction* $\bigvee$, the *unique* connective U, the *majority* connective *Maj*, for $c \in \mathbb{N}$ the *c-threshold* connectives $c_>$ and $c_\leq$, the *not-all-equal* connective *NAE* defined by[2]

$$\bigwedge(m,n) = 1 \iff n = 0; \qquad \bigvee(m,n) = 1 \iff m \neq 0;$$
$$U(m,n) = 1 \iff m = 1; \qquad \mathit{Maj}(m,n) = 1 \iff m > n;$$
$$c_>(m,n) = 1 \iff m < c; \qquad c_\leq(m,n) = 1 \iff c \leq m;$$
$$\mathit{NAE}(m,n) = 1 \iff m \geq 1 \text{ and } n \geq 1.$$

[2]Whenever we write $C(m, n)$ we assume that $m + n \geq 1$.

Finally, we define the *(big) negation* $\neg$ (we denoted this connective by C_0 in Section 1) by ($\neg(m,n) = 1 \iff m = 0$).

Let $\mathcal{C}$ be a finite set of connectives (throughout this paper $\mathcal{C}$ will always denote a *finite* set of connectives). A $\mathcal{C}$*-circuit* D is a finite connected acyclic directed graph with multiple edges; mostly we will call the vertices of D *gates*. Each gate of D of positive fan-in is labelled with a symbol $C \in \mathcal{C}$. We then call it a C-gate.

Gates with fan-in zero are the *input gates*; they are labeled with *variables* X_1,$X_2, \ldots$ or with the *Boolean constants* $\top$ and $\bot$. We only consider circuits having exactly one gate of fan-out zero, the *output gate*. We let $X, Y, Y_1, Y_2, \ldots, Z$ denote variables. We denote by CIRC($\mathcal{C}$) the class of all $\mathcal{C}$-circuits.

A *Boolean* circuit is a $\{\neg, \bigwedge, \bigvee\}$-circuit. Throughout this paper we consider that $\neg$-gates have fan-in one.

The size $\|D\|$ of a $\mathcal{C}$-circuit D is (number of gates of D + number of egdes of D).

An *assignment* or *valuation* for a $\mathcal{C}$-circuit D is a mapping $\mathcal{V}$ from a set of variables containing all the variables occurring in D to $\{1, 0\}$. In the obvious bottom-up way one defines the value $\mathcal{V}(g)$ for any gate g of D, the main clause being:

> If g is labelled by C and has entries from the gates $(g_i)_{i\in I}$ (where a gate g' occurs m times in the enumeration $(g_i)_{i\in I}$ if there are exactly m edges from g' to g), then
>
> $$\mathcal{V}(g) := C(|\{i \in I \mid \mathcal{V}(g_i) = 1\}|,\ |\{i \in I \mid \mathcal{V}(g_i) = 0\}|).$$

The assignment *satisfies* the circuit if its value for the output gate is 1. A $\mathcal{C}_1$-circuit D_1 and a $\mathcal{C}_2$-circuit D_2 are *equivalent*, $D_1 \equiv D_2$, if they are satisfied by the same assignments defined on at least all variables occurring in D_1 or D_2.

The *weight* of an assignment is the number of variables set to 1. A circuit D is k*-satisfiable* (where $k \in \mathbb{N}$), if there is an assignment for the input variables of D of weight k satisfying D. For a set Ω of $\mathcal{C}$-circuits, the *parameterized weighted satisfiability problem* p-WSAT(Ω) *for circuits in* Ω is the following problem:

p-WSAT(Ω)	
Input:	A circuit $D \in \Omega$ and $k \in \mathbb{N}$.
Parameter:	k.
Question:	Is D k-satisfiable?

A $\mathcal{C}$-circuit where all gates, besides the output gate, have fan-out one is a $\mathcal{C}$-*formula*. They constitute the formulas of *propositional logic with connectives from* $\mathcal{C}$. Thus these formulas can be viewed as the strings obtained from the propositional variables $X_1, X_2, \ldots$ and the constants $\top$ and $\bot$ by finitely many applications of the rule:

If $n \in \mathbb{N}$ and $\alpha_1, \ldots, \alpha_n$ are $\mathcal{C}$-formulas and $C \in \mathcal{C}$, then $C[\alpha_1, \ldots, \alpha_n]$ is a $\mathcal{C}$-formula.

We denote by FORM($\mathcal{C}$) the class of all $\mathcal{C}$-formulas.

Definition 2. *A connective C is* bounded *if there is a $b \in \mathbb{N}$ such that for all $m, n, n' \in \mathbb{N}$ with $n, n' \geq b$*

$$C(m, n) = C(m, n') \qquad \textit{and} \qquad C(n, m) = C(n', m).$$

*We then say that C is b-*bounded*. Clearly, if C is b-bounded and $b < b'$, then C is b'-bounded. The smallest b such that C is b-bounded is denoted by $b(C)$.*

Example 3. *The reader will easily verify that Maj is not bounded and that*

$$b(\neg) = b(\bigwedge) = b(\bigvee) = b(\mathit{NAE}) = 1, \quad b(U) = 2, \quad b(c_>) = b(c_\leq) = c.$$

Weft and the W-hierarchy. Let $\mathcal{C}$ be a set of bounded connectives. Let D be a $\mathcal{C}$-circuit. A C-gate of D is *small* if it has fan-it less than $2(b(C) + 1)$; otherwise it is *large*. A circuit is *small* if it only contains small gates. The *weft* of D is the maximum number of large gates on any path from the input gates of D to its output gate. The *depth* of D is the maximum number of (large and small) gates of positive fan-in on any path from the input gates of D to its output gate. We set

$$\Omega_{t,d}(\mathcal{C}) := \{D \mid \ D \text{ a } \mathcal{C}\text{-circuit of weft} \leq t \text{ and depth} \leq d.\}$$

By definition , for $t \geq 1$, W$[t]$ is the class of parameterized problems fpt-reducible to p-WSAT$(\Omega_{t,d}(\{\neg, \bigwedge, \bigvee\}))$ for some $d \in \mathbb{N}$. [3] The classes W$[1]$, W$[2], \ldots$ constitute the W-hierarchy. Furthermore W[SAT] and W[P] are the class of parameterized problems that are fpt-reducible to the problem p-WSAT(FORM$(\{\neg, \bigwedge, \bigvee\})$) and to the class of problems reducible to p-WSAT(CIRC$(\{\neg, \bigwedge, \bigvee\})$). Therefore we define:

Definition 4. *Let $\mathcal{C}$ be a class of connectives.*

- *W[SAT]($\mathcal{C}$) is the class of parameterized problems fpt-reducible to the problem p-*WSAT(FORM($\mathcal{C}$))*;*
- *W[P]($\mathcal{C}$) is the class of parameterized problems fpt-reducible to the problem p-*WSAT(CIRC($\mathcal{C}$)).

Let $\mathcal{C}$ be a class of bounded connectives.

[3] Recall the notions of parameterized problem and of fpt-reduction from [4]. Note that in [4] the depth is defined without taking into account the $\neg$-gates. Clearly, this difference has no effect on the definition of W$[t]$.

- *For* $t \geq 1$, $\mathrm{W}[t]$*($\mathcal{C}$) is the class of parameterized problems fpt-reducible to* p-$\mathrm{WSAT}(\Omega_{t,d}(\mathcal{C}))$ *for some* $d \in \mathbb{N}$*. The classes* $\mathrm{W}[1](\mathcal{C}), \mathrm{W}[2](\mathcal{C}), \ldots$ *constitute the W($\mathcal{C}$)*-hierarchy.

Clearly, for a class $\mathcal{C}$ of bounded connectives, we have

$$\mathrm{W}[1](\mathcal{C}) \subseteq \mathrm{W}[2](\mathcal{C}) \subseteq \cdots \subseteq \mathrm{W}[\mathrm{SAT}](\mathcal{C}) \subseteq \mathrm{W}[\mathrm{P}](\mathcal{C}).$$

3 Comparing the W-hierarchy and the W$(\mathcal{C})$-hierarchy for classes $\mathcal{C}$ of bounded connectives.

We show that the W-hierarchy and the W$(\mathcal{C})$-hierarchy coincide levelwise for a set of bounded connectives $\mathcal{C}$ satisfying some further conditions.

Theorem 5. If $\mathcal{C}$ is a set of bounded connectives, then

$$\mathrm{W}[t](\mathcal{C}) \subseteq \mathrm{W}[t] \text{ for all } t \geq 1\,, \quad \mathrm{W}[\mathrm{SAT}](\mathcal{C}) \subseteq \mathrm{W}[\mathrm{SAT}], \quad \mathrm{W}[\mathrm{P}](\mathcal{C}) \subseteq \mathrm{W}[\mathrm{P}].$$

This result is proved in the full paper, due to the space limitations for this extended abstract. The proof is based on the following two facts holding for every bounded connective C:

- For $m, n \geq b(C)$ we have $C(m,n) = C(b(C), b(C))$.
- A C-gate with fan-in less than $2 \cdot (b(C)+1)$ can be simulated by a small Boolean circuit of constant depth.

For the last inclusion of the preceding theorem we do not need the boundedness of the connectives in $\mathcal{C}$, that is (see Appendix **??** for a proof):

Proposition 6. If $\mathcal{C}$ is a set of connectives, then W[P]$(\mathcal{C}) \subseteq$ W[P].

For converse inclusions we look for conditions on $\mathcal{C}$ that allow us to find a weft preserving translation from Boolean circuits to $\mathcal{C}$-circuits.

Definition 7. *Let C be a connective.*

- C *is* $\neg$-closed *if and only if there are* $m, n, r \in \mathbb{N}$ *such that*

$$0 = C(m+r, n) \neq C(m, n+r) = 1.$$

- C *is* $\bigvee$-closed *if and only if there are* $m, n \in \mathbb{N}$ *such that for all* $r \geq 1$ *and* $s \in [r]$

$$C(m, n+r) \neq C(m+s, n+r-s).$$

- C *is* monotone *if and only if* $C(m,n) \leq C(m+r, n-r)$ *for all* $m, n \in \mathbb{N}$ *and all* $r \in [n]$.

Example 8. *(a) $c_{\leq}$ and Maj are monotone. No monotone connective is $\neg$-closed; in particular, $c_{\leq}$ and Maj are not $\neg$-closed.*

(b) The connectives NAE, U, and $c_{>}$ are $\neg$-closed and the connectives NAE, U, $c_{>}$, and $c_{\leq}$ are $\bigvee$-closed (details in the full paper).

We say that a class $\mathcal{C}$ of connectives is *$\neg$-closed* if at least one connective in $\mathcal{C}$ is *$\neg$-closed*. Similarly, $\mathcal{C}$ is *$\bigvee$-closed* if at least one connective in $\mathcal{C}$ is *$\bigvee$-closed*. We show in the full paper:

Theorem 9. Let $\mathcal{C}$ be a $\neg$-closed and $\bigvee$-closed set of bounded connectives. Then

$$\mathrm{W}[t] = \mathrm{W}[t](\mathcal{C}) \text{ for all } t \geq 1\,, \quad \mathrm{W[SAT]} = \mathrm{W[SAT]}(\mathcal{C}), \quad \mathrm{W[P]} = \mathrm{W[P]}(\mathcal{C}).$$

For the last equality, we do not need the boundedness of the connectives.

Corollary 10. The W-hierarchy and the $\mathrm{W}(\mathcal{C})$-hierarchy coincide levelwise and the classes W[SAT] and W[SAT] $(\mathcal{C})$ and the classes W[P] and W[P] $(\mathcal{C})$ coincide

- for $\mathcal{C} = \{\neg, \bigwedge, \bigvee, \mathit{NAE}, U, c_{1>}, \dots, c_{s>}, c'_{1\leq}, \dots, c'_{r\leq}\}$, where $s, r \in \mathbb{N}$ and $c_1, \dots, c_s, c'_1, \dots, c'_r \geq 1$.
- for $\mathcal{C} = \{\mathit{NAE}\}$, $\mathcal{C} = \{U\}$, and $\mathcal{C} = \{c_{>}\}$, where $c \geq 1$.

4 The Threshold Connectives $c_{\leq}$

In the following, for $\mathcal{C} = \{C\}$, we often write C-circuit instaed of $\mathcal{C}$-circuit and use analogous conventions for other notions.

From Section 2, we know that the threshold connectives of the form $c_{\leq}$ with $c \geq 1$ are monotone and bounded. By the second property, we get from Theorem 5

$$\mathrm{W}[t](c_{\leq}) \subseteq \mathrm{W}[t]$$

for all $t \geq 1$. However, we can even show that $\mathrm{W}[t](c_{\leq})$ is contained in PTIME (details in the full paper):

Theorem 11. Let $c, d \geq 1$. There is a polynomial time algorithm that, given a $c_{\leq}$-circuit D of depth $\leq d$ and $k \in \mathbb{N}$ decides whether D is k-satisfiable.

The previous result shows that, for $\mathcal{C} = \{c_{\leq}\}$, the W-hierarchy and the W($\mathcal{C}$)-hierarchy do not coincide levelwise; however, W[P] and W[P]($\mathcal{C}$) coincide as shown by Theorem 12 below. We formulate this theorem (proved in the full paper) in such a way that it yields weighted satisfiability problems of $c_{\leq}$-circuits complete for the classes $\mathrm{W}[1]$, W[SAT], and W[P].

Let $f : \mathbb{N} \times \mathbb{N} \to \mathbb{N}$ be a computable function. The *weighted satisfiability problem p-*WSAT$(c_{\leq}, f)$ *of $c_{\leq}$-circuits of depth f* is given by

p-WSAT$(c_{\leq}, f)$	
Input:	$k \in \mathbb{N}$ and a pure $c_{\leq}$-circuit D of depth $\leq f(k, \|D\|)$.
Parameter:	k.
Question:	Does $\mathcal{C}$ have a satisfying assignment of weight k?

With p-WSAT(small $c_{\leq}$; f) we denote the corresponding problem where the input circuit is required to be small in addition.

Theorem 12. Let $c > 1$.

(a) p-WSAT(CIRC$(c_{\leq})$) is W[P]-complete under fpt-reductions.

(b) For sufficiently large d the problem p-WSAT(small $c_{\leq}$; $d \cdot \log n$) (more precisely, the problem p-WSAT(small $c_{\leq}$; f), where $f(k, n) := d \cdot \log n$) is W[SAT]-complete under fpt-reductions.

(c) Let f be a computable function depending only on the first argument (that is, $f(k, n) = g(k)$ for some computable g) and assume that $f(k, n) \geq 2 + 2 \log k$ for all $k \in \mathbb{N}$. Then p-WSAT$(c_{\leq}, f)$ is W[1]-complete under fpt-reductions.

5 The Majority Connective

We have seen that the majority connective *Maj* is neither bounded nor $\neg$-closed. In particular, the notion of small *Maj*-gate is not defined so far. As

(2) $\quad (Y_1 \wedge Y_2) \equiv \textit{Maj}[Y_1, Y_2] \quad$ and $\quad (Y_1 \vee Y_2) \equiv \textit{Maj}[\top, Y_1, Y_2],$

it seems to be natural to identify *small Maj*-gates with *Maj*-gates of fan-in less than or equal to three. Furthermore, we have:

(3) $$\bigvee_{i \in [n]} Y_i \equiv \textit{Maj}[Y_1, \ldots, Y_n, \underbrace{\top, \ldots, \top}_{n \text{ times}}]; \quad \bigwedge_{i \in [n]} Y_i \equiv \textit{Maj}[Y_1, \ldots, Y_n, \underbrace{\bot, \ldots, \bot}_{n-1 \text{ times}}].$$

Finally, for pairwise distinct variables $Y_1, \ldots, Y_n$ and $i \in [n]$ the following formulas are satisfied by the same assignments of weight k to these variables, where $2k \leq n$,

(4) $$\neg Y_i \quad \text{and} \quad \textit{Maj}[Y_1, \ldots, Y_{i-1}, Y_{i+1}, \ldots, Y_n, \underbrace{\top, \ldots, \top}_{n-1-2k+2 \text{ times}}].$$

In general, the *Maj*-gate in the formula on the right hand side will be large. Using these equivalences one gets (details in the full paper):

Theorem 13. W[P]=W[P](*Maj*).

In order to prove our next claim we consider the problem p-MAJORITY-VERTEX-COVER defined in Section 1, which given a graph and a natural number k asks for a set of k vertices covering the majority of the edges. Even though the parameterized vertex cover problem is fixed-parameter tractable, we will show the $\mathrm{W}[1]$-completeness of this variant. First we obtain:

Lemma 14.

(a) p-MAJORITY-VERTEX-COVER $\in \mathrm{W}[1]$(*Maj*).

(b) p-MAJORITY-VERTEX-COVER is $\mathrm{W}[1]$-hard under fpt-reductions.

Proof. Let (G, k) be an instance of p-MAJORITY-VERTEX-COVER. We construct a *Maj*-circuit D of weft 1 and depth 2 such that

$$(G, k) \in p\text{-MAJORITY-VERTEX-COVER} \iff D \text{ is } k\text{-satisfiable}. \tag{5}$$

Let $G = (V, E)$ and $n = |V|$ and $m = |E|$. The set V together with an additional gate will be the set of input gates of D; vertex v is labelled by a variable X_v and the additional gate by $\top$. Beyond these input gates we have a level of *Maj*-gates of fan-in 3, one for each edge $e \in E$. The gate associated with the edge $e = \{u, v\}$ is connected to the gates u, v and the gate labelled by $\top$. Note that all these *Maj*-gates are small and each of them is satisfied by an assignment if and only if the edge associated with this gate is incident to at least one vertex selected by the assignment. Finally the circuit D has as output a further *Maj*-gate which receives its input from all the small *Maj*-gates.

One easily verifies that (5) holds and thus $(G, k) \mapsto (D, k)$ is an fpt-reduction from p-MAJORITY-VERTEX-COVER to p-WSAT($\Omega_{1,2}$(*Maj*)); hence the former problem is in $\mathrm{W}[1]$(*Maj*).

We obtain part (b) by reducing the $\mathrm{W}[1]$-complete problem parameterized independent set problem p-INDEPENDENT-SET to p-MAJORITY-VERTEX-COVER (details in the full paper). ■

By this lemma we know that $\mathrm{W}[1] \subseteq \mathrm{W}[1]$(*Maj*). We can even show that the two classes coincide. For $t > 1$ we only get the inclusion and we conjecture that this inclusion is strict, $\mathrm{W}[t] \subset \mathrm{W}[t]$(*Maj*) for $t > 1$.

Theorem 15. $\mathrm{W}[1] = \mathrm{W}[1]$(*Maj*) and $\mathrm{W}[t] \subseteq \mathrm{W}[t]$(*Maj*) for $t > 1$.

This result is proven in the full paper. Together with the previous lemma, we get:

Corollary 16. p-MAJORITY-VERTEX-COVER is $\mathrm{W}[1]$-complete under fpt-reductions.

6 Conclusions

We have seen (cf. Theorem 5) that in revisiting the original definition of the W-hierarchy by means of Boolean circuits (*large* and *small*), we can explore the concept of *circuit weft* (or more simply, *large gate depth*, in the context of overall bounded depth) by considering gates labelled by arbitrary bounded connectives. The majority connective is not bounded, nevertheless the first level of the corresponding hierarchy coincides with $\mathrm{W}[1]$. For higher levels we only know that $\mathrm{W}[t] \subseteq \mathrm{W}[t](\mathit{Maj})$. There are various open questions related to the question whether these classes are distinct. For example, let us consider the majority versions of the $\mathrm{W}[2]$-complete parameterized dominating set problem p-DS and of the hitting set problem p-HS.

p-MAJ-DS	
Input:	A graph G and $k \in \mathbb{N}$.
Parameter:	k.
Question:	Does G have a set of k vertices dominating the majority of vertices?

p-MAJ-HS	
Input:	A hypergraph H and $k \in \mathbb{N}$.
Parameter:	k.
Question:	Does H have a set of k vertices hitting the majority of hyperedges?

Here a set S of vertices in a graph $G = (V, E)$ *dominates* a vertex u if $u \in S$ or there is a $v \in S$ such that $\{u, v\} \in E$. A set S of vertices in a hypergraph $H = (V, E)$ *hits* an hyperedge $e \in E$ if $S \cap e \neq \emptyset$.

What we know about the relationship between these problems is contained in the following theorem proven in the full paper:

Theorem 17.

(a) p-DS $\leq^{\text{fpt}}$ p-MAJ-DS $\equiv^{\text{fpt}}$ p-MAJ-HS.

(b) p-MAJ-HS $\in \mathrm{W}[2](\mathit{Maj})$.

We close by mentioning two open problems in connection with the previous theorem explicitly:

- Is p-MAJ-DS $\leq^{\text{fpt}}$ p-DS?
- Is p-MAJ-HS hard under fpt-reductions for the class $\mathrm{W}[2](\mathit{Maj})$?

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